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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
MASKULINSKI, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2113	7

DATE MAILED: 05/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/846,868	Applicant(s) CHAN, JONG	
	Examiner Michael C Maskulinski	Art Unit 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Second Non-Final Office Action

Claim Objections

1. In view of the recent amendments, the claim objections have been withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 37-46 are rejected under 35 U.S.C. 102(b) as being anticipated by McLaughlin et al., U.S. Patent 5,202,822.

Referring to claim 37:

a. In column 2, lines 7-11, McLaughlin et al. disclose a controller which operates as a master, and a slave input/output processor (IOP) connected thereto which communicates with at least one device of a predetermined type, the types including analog input, analog output, digital input, and digital output (providing a plurality of control units, each control unit having a capability to control the transfer of data between the data processor and the data unit). Further, in Figure 3, McLaughlin et al. disclose each control unit having a memory device and signal paths coupled to the memory device, the signal paths enabling access to the associated memory device.

b. In column 2, lines 7-11, McLaughlin et al. disclose a controller, which operates as a master (selecting one of the control units as a master control unit to control transfer of data between the data processor and the data unit).

c. In column 2, lines 7-11, McLaughlin et al. disclose a slave input/output processor (IOP) (designating a second one of the control units as a slave control unit).

d. In column 4, lines 53-59, McLaughlin et al. disclose a local memory stores information, including personality image which is downloaded from the plant control network and a global memory that stores information which is common to both processor A and processor B. It also stores all the data received from Bus A and Bus B (transferring the data between the data processor and the data unit by employing the memory device in the master control unit).

e. In column 2, lines 14-21, McLaughlin et al. disclose that the slave IOP is operatively connected to the device and operates as a primary IOP to the device. A method for providing backup to the slave IOP by the backup slave IOP comprises the steps of loading the backup slave IOP with the same data base as the slave IOP. The backup slave IOP eavesdrops on all communications from the controller to the slave IOP (synchronizing the memory device in the master control unit with the memory device in the slave control unit, the synchronizing including: generating, in the master control unit, values for the signal paths associated with the master memory device to transfer data to the master memory device; transferring a subset of the generated signal paths to the signal paths

associated with the slave memory device; and allowing the generated signals to perform the data transfer to the master memory device and the slave memory device).

Referring to claim 38, in column 8, lines 12-24, McLaughlin et al. disclose that the controller acts to synchronize the IOP(B). Synchronizing is the process whereby the same data base is contained in both IOP(A) and IOP(B). The information of the data base of IOP(A) is requested by the controller and then transferred to IOP(B) thereby causing the data base of IOP(B) to be the same, whereupon IOP(B) is commanded to start executing. IOP(B) performs the same operations as IOP(A) and outputs the same information to the FTA at essentially the same time (each IOP is operating off its own clock). It will be recognized that IOP(B) is a dedicated backup (generating, in the master control unit, values for the signal paths associated with the slave memory device that enables access to the slave memory device).

Referring to claim 39, in TABLE 1, in column 8, McLaughlin et al. teach associating an address and control signal path with each memory device that enables access to the corresponding memory device. Further, in column 8, lines 26-33, McLaughlin et al. disclose that once IOP(B) is synchronized, the controller data base is updated as shown in state 3 of Table 1. In normal operation, all transfers (i.e., writes) to the IOP(A) 21-A from controller 30 are also received by IOP(B). IOP(B) eavesdrops on the communications since both IOP(A) and IOP(B) have a logical address of 1 in this example and the controller 30 communicates to the IOPs by logical address (producing values for the address and control signal paths associated with the master memory

device and transmitting the address and control signal paths associated with the master memory device to the address and control signal paths associated with the slave memory device).

Referring to claim 40, in column 8, lines 26-33, McLaughlin et al. disclose that once IOP(B) is synchronized, the controller data base is updated as shown in state 3 of Table 1. In normal operation, all transfers (i.e., writes) to the IOP(A) 21-A from controller 30 are also received by IOP(B) (associating with the master memory device a first control signal that controls access to the slave memory device). IOP(B) eavesdrops on the communications since both IOP(A) and IOP(B) have a logical address of 1 in this example and the controller 30 communicates to the IOPs by logical address (associating with each memory device a second control signal that controls access to the corresponding memory device). Further, in column 8, lines 12-33, McLaughlin et al. teach producing values for the first control signal and the second control signal associated with the master memory device and transmitting the first control signal associated with the master memory device to the second control signal associated with the slave memory device).

Referring to claim 41, in column 8, lines 26-33, McLaughlin et al. disclose that once IOP(B) is synchronized, the controller data base is updated as shown in state 3 of Table 1. In normal operation, all transfers (i.e., writes) to the IOP(A) 21-A from controller 30 are also received by IOP(B) (associating with the master memory device a first control signal that controls access to the slave memory device). IOP(B) eavesdrops on the communications since both IOP(A) and IOP(B) have a logical address of 1 in this

example and the controller 30 communicates to the IOPs by logical address (receiving data values for the data signal path associated with the master memory device and transmitting the received data values to the data signal path associated with the slave memory device).

Referring to claim 42, in column 8, lines 26-33, McLaughlin et al. disclose that once IOP(B) is synchronized, the controller data base is updated as shown in state 3 of Table 1. In normal operation, all transfers (i.e., writes) to the IOP(A) 21-A from controller 30 are also received by IOP(B) (associating with the master memory device a first control signal that controls access to the slave memory device). IOP(B) eavesdrops on the communications since both IOP(A) and IOP(B) have a logical address of 1 in this example and the controller 30 communicates to the IOPs by logical address. Further, in column 8, lines 60-63, McLaughlin et al. disclose that when an error is detected, it is desired that IOP(A) no longer communicate to the field devices, and that the IOP(B) pick up communications essentially immediately. This switching is referred to as failover (associating with the signal paths associated with each memory device a control mechanism that enables a transfer of values from a first signal path to a second signal path; and enabling the control mechanism associated with the master memory device and the control mechanism associated with the slave memory device to transfer values between the master signal paths and the slave signal paths).

Referring to claim 43, in column 8, lines 60-63, McLaughlin et al. disclose that when an error is detected, it is desired that IOP(A) no longer communicate to the field devices, and that the IOP(B) pick up communications essentially immediately. This

switching is referred to as failover (disabling the control mechanism associated with a memory device to inhibit a transfer and receipt of signal paths values).

Referring to claim 44, in column 9, lines 1-9, McLaughlin et al. disclose that control lines A are connected from IOP(A) to switching module, and control lines B are connected from IOP(B) to switching module. The switching module controls the arm of relay. The switching module includes logic, which detects and responds to control signals on control lines 260-A, 260-B and causes the relay to switch to the "B" terminals (suspending the master control unit from controlling the data transfer between the data processor and the data unit; enabling the slave control unit the transfer of data between the data processor and the data unit; and transferring the data between the data processor and the data unit by employing the memory device in the slave control unit).

Referring to claim 45, in column 8, lines 60-63, McLaughlin et al. disclose that when an error is detected, it is desired that IOP(A) no longer communicate to the field devices, and that the IOP(B) pick up communications essentially immediately. This switching is referred to as failover (determining that the master control unit has experienced an operational fault).

Referring to claim 46, in column 8, lines 63-67, McLaughlin et al. disclose that failures can be detected by internal microprocessors failing self-tests, parity errors, watch-dog times timing out, etc. Failures can also be directed by the controller in detecting a condition undetected by the primary IOP (receiving an indication that the memory device in the master control unit has failed).

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over McLaughlin et al., U.S. Patent 5,202,822 as applied to claim 37 above, and further in view of Kern et al., U.S. Patent 5,734,818.

Referring to claims 47 and 48, in column 4, lines 16-22, McLaughlin et al. disclose that one controller operates as a primary controller and the other controller operates as a secondary controller in more of a reserved mode than a back-up, in that if a failure of controller A should occur, controller B is ready to take over the control function with essentially no startup or initialization time. However, McLaughlin et al. don't explicitly disclose disabling the master control unit from accessing the slave memory device and suspending operation of the slave unit because the slave control unit has experienced an operational failure. In column 7, lines 56-67 continued in column 8, lines 1-5, Kern et al. disclose that in the case that the duplex pair is in a "failed" state, then the primary storage controller notifies the primary processor that the duplex pair has suspended or failed. Further, in column 5, lines 58-67 continued in column 6, lines 1-7, Kern et al. disclose that the primary site may break the duplex pair if the primary site is unable to write updated data to the secondary site. It would have been obvious to one of ordinary skill at the time of the invention to include the detection of an error in the slave device and suspension of the device in response to the error of Kern et al. into the system of McLaughlin et al. A person of ordinary skill in the art would have been motivated to make the modification because a failed device can

corrupt data or it can cause further errors by not being accessible by the master device. Further, if the failure is in the communication link, then the primary storage controller is unable to communicate the failure directly to the secondary storage controller. Therefore, disconnection of the secondary storage controller is necessary (see Kern et al.: column 7, lines 63-66).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (703) 308-6674. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100